3800 TSD Electronics Circuit Description
Revision: 1
Date: September 12, 1995

1. Applicability

This document applies to Mercury TSD schematic 03-925073-01, Revision C1.

2. Power supplies and grounds

There are four grounds serving the TSD electronics circuitry. Ground 1 is the return for the +5V digital supply. It is connected directly to Ground 4, the unregulated +24V return, at the card edge connector on the Mother board. The analog return is Ground 2, which provides a low-noise return for the ±15V, -5V, and +5.25V supplies. Ground 3 is the reference for analog signal distribution, which carries almost no DC current. All of the grounds must be tied together externally for the board to function properly.

Four RC filters remove noise from the analog power supplies. These consist of R13 with C16, R12 with C15, R10 with C13, and R11 with C14.

3. Digital circuits

U4 decodes bus address information to access latch U3, DAC U6, and buffer U2. The latch holds all of the digital control signals for the board, while the buffer transmits the board identification number and serial data from EEPROM U5 to the bus. R18 and R20 set the desired operating logic levels, while allowing the inputs to be pulled high or low for test purposes.

The EEPROM is a 1024-bit device which is used to store calibration data. Software has full control over the serial interface, consisting of the chip select, shift clock, and data inputs (pins 1 - 3, respectively), and must reassemble the stored data from the serial output stream coming from pin 4. When the EEPROM is not selected, its output is high impedance. R19 provides a positive level to CMOS buffer U2 in this case.

4. Input log amplifier of square-root electrometer

The electrometer is a multi-stage circuit which produces an output voltage that is proportional to the square-root of the input current. This is accomplished by three amplifier stages, AR1 (dual) and AR2, having logarithmic and exponential responses. The nonlinear responses are generated by the fundamental characteristic of bipolar transistors, which is represented in the following equations:

$v_{be} = (nkT/q) \log(I_c/I_{sat} + 1)$ or $I_c = I_{sat} (e^{(qv_{be}/nkT)} - 1)$,

where v_{be} = base-emitter voltage (volts)
n = emission coefficient (near 1.00)
k = Boltzmann's constant (1.38E-23 Joule/K)
T = Temperature (Kelvins)
q = electron charge (1.6E-19 coulomb)
I_c = collector current
I_{sat} = saturation current
e = base of natural logarithms

Input amplifier AR2 has an extremely high input impedance, with a bias current of only about 40fA (40 x 10^{-15}A). All of the input current from J1 must therefore be supplied from the collector of Q1 (pin 8). Negative feedback from the output of AR2 adjusts the base-emitter voltage of Q1 until precisely this current flows into the collector. The output voltage from this stage, which is taken from the emitter of Q1 (pin 6), is therefore $v_{eb1} = (nkT/q) \log(I_{in}/I_{sat} + 1)$. R4 stabilizes the loop gain at input currents near full scale (1μA), where the impedance looking into the emitter of Q1 has dropped to 26k.

Since the non-inverting input of AR2 is grounded, the inverting input remains at ground also, keeping the collector of Q1 at ground. This holds the collector-base voltage at zero, which is a necessary condition for the equations above to apply. The input connection at J1 also remains near ground at low input currents, minimizing noise due to variations in input capacitance. R1 limits input current if an excessive voltage is applied to the input, but it also allows the input voltage to rise slightly at the higher input currents. R2, which isolates the amplifier input from the input cable capacitance for loop stability, has almost no DC voltage drop across it, since only the bias current of AR2 flows through it. C3 also enhances loop stability, and reduces high-frequency noise.

Because of the high impedance levels, this entire circuit must be shielded to work properly at all but the highest input currents. It is also easily upset by test probes even when shields are in place. In any case, the exact output voltage to be expected at a particular input current is unknown, since the saturation current of the input log transistor is unknown. All that can be predicted is that the output voltage will increase (in a positive direction) by about 26mV when the input current is doubled, or by 60mV when the input current is raised by ten times, regardless of the specific current levels.

5. Reference current log amplifier

The saturation currents of the individual transistors vary from one unit to the next, and also change rapidly with temperature, doubling with each 10°C rise. In order to maintain stable and predictable calibration, each transistor used in the anti-log stage must be balanced by a matching transistor in a log stage. The anti-log stage uses two transistors, as will be described below, so a second log amplifier is needed for compensation purposes. This stage consists of one section each of AR1 (pins 1-3) and Q2 (pins 6-8), and is very similar to the input log amplifier. AR4 (pins 5-7) inverts the +10V reference voltage to produce the negative reference current needed by this stage.

The sum of the two emitter-base voltages of the log transistors is produced directly by connecting them in series. The emitter of Q1 (pin 6) is connected to the base of the Q2 (pin 7), and the output v_{sum} is taken from the emitter of Q2 (pin 6). The collector of Q2 (pin 8) is connected to the inverting input of AR1 (pin 2), which is held at the same voltage as the noninverting input (pin 3). By connecting the base of Q2 (pin 7) to the noninverting input, the collector-base voltage is forced to be zero. This causes the inverting input to follow the output voltage of AR2 (pin 1). The temperature drift of this voltage is compensated by CR1, which keeps the reference current relatively constant as the temperature changes. As this voltage varies by a few hundred millivolts over the full range of the input current, the reference current (I_{ref}) through R5 varies between 23 and 24 microamps. The emitter-base voltage of Q2 is thus $v_{eb2} = (nkT/q) \log(I_{ref}/I_{sat} + 1)$, and the net voltage at the emitter of Q2 is

$$v_{sum} = (nkT/q) \log(I_{in}/I_{sat} + 1) + (nkT/q) \log(I_{ref}/I_{sat} + 1)$$

$$= (nkT/q) \log ((I_{in}/I_{sat} + 1)(I_{ref}/I_{sat} + 1)).$$

AR1 is powered from the ±15V power supplies, which could cause avalanche breakdown of the emitter-base junction of Q2, if the amplifier output ever approached the negative supply voltage. While this never occurs in normal operation, even a momentary breakdown can cause a permanent increase in saturation current. CR2 prevents the emitter voltage from rising to a destructive level during testing or other transient fault conditions.

6. Anti-log amplifier

The logarithmically compressed voltage v_{sum} is applied to an anti-log (or exponential) amplifier stage which utilizes the other halves of matched dual transistors Q1 and Q2. Since the anti-log transistors are connected in series, both collector currents are essentially equal. If we assume that all of the transistors are at the same temperature T and have the same saturation current I_{sat}, the base-emitter voltage of each of the anti-log transistors will be half the value of v_{sum}. Their collector currents must then be $I_c = I_{sat} (e^{-(qv_{sum}/2nkT)} - 1)$ from the equation in section 4. Substituting the expression for v_{sum} above, we have

$$I_c = I_{sat}\,(e^{(1/2)\log((Iin/Isat + 1)(Iref/Isat + 1))} - 1)$$

$$= I_{sat}\,(\mathrm{sqrt}((Iin/Isat + 1)(Iref/Isat + 1)) - 1)$$

$$= \mathrm{sqrt}((I_{in} + I_{sat})(I_{ref} + I_{sat})) - I_{sat}$$

$$= \mathrm{sqrt}((I_{in} + I_{sat})(I_{ref})) - I_{sat} \qquad (\text{since } I_{ref} > 10^9 \text{ x Isat})$$

Amplifier AR1 holds the collector of Q1 (pin 1) at ground potential and forces the collector current to flow through R3. The final output voltage at P1-1 is then

$$v_{out} = 2.05 \text{ x } 10^6 \text{ x } \mathrm{sqrt}((I_{in} + I_{sat})(I_{ref})) + v_{os},$$

where v_{os} is the sum of the input offset voltage of AR1 and all of the current-related voltage errors. Putting in the nominal value of 25 microamps for I_{ref} gives the following approximate formula for the output voltage:

$$v_{out} = 10^4 \text{ x } \mathrm{sqrt}(I_{in} + I_{sat}) + v_{os}.$$

This formula will not be accurate if the temperatures of all of the transistors are not equal. The two halves of each dual transistor are always at the same temperature, since they are fabricated on a single silicon die. Q1 and Q2 track each other in temperature only by being in close proximity in an isolated environment, however, and any thermal disturbance will cause the output of the electrometer to drift. Simply touching one of the transistors can cause a minute or two of drift, and the output may not stabilize for 5 or 10 minutes after soldering in the vicinity of the transistors.

The time constant of the amplifier is set to 45ms by C1, and C2 eliminates high-frequency noise from digital sources. R7 and C12 prevent glitches from the ADC multiplexer (on the main system board), which reads the output voltage of the electrometer, from disturbing the amplifier output. Such glitches can couple through C1 and the capacitance between the collectors of the two halves of Q1 to disturb the sensitive input node, resulting in a much longer settling time than would be expected.

7. Electrometer diagnostic features

In order to determine the input current from the output voltage, the value of v_{os} in the equation in the preceding paragraph must be determined. This is done during operation by closing the switch section of U1 (pins 1-3) which is connected to the output of the reference log amplifier. Current through the anti-log transistors is thus cut off, leaving the output voltage at P1-1 equal to v_{os}.

Though it is not immediately obvious from the equations presented here, closing the switch section of U1 (pins 14-16) which is connected to the output of the input log

amplifier results in an output voltage at P1-1 which corresponds to an input current equal to the saturation current of Q1. This measurement is used for diagnostic purposes only. Both of the diagnostic switch sections of U1 are left open in normal operation.

Because the input stage of the electrometer has a logarithmic response, its behavior becomes unpredictable as the input current approaches zero. All of the voltages applied to the circuit are above ground potential, so leakage currents should never cause the input to reverse in polarity and saturate the output positively. However, the response time of the circuit is inversely proportional to the current level, becoming very slow at currents below a few hundred femtoamps. For this reason, it is impractical to test the noise and drift of the electrometer by "capping off" the input with no input current.

To test the electrometer when no external picoamp source is available, an input current source in the picoampere range has been provided. This source relies upon the fact that the current through a capacitor is equal to the product of the capacitance and the rate of change of the voltage across the capacitor. C4 (10pF) is connected to the electrometer input, which remains near ground potential. Applying a negative sawtooth waveform to the other end of C4 should thus produce a steady input current, with positive spikes on the positive transitions of the sawtooth voltage. This waveform (modified somewhat to optimize the recovery of the electrometer from the positive spikes) is generated by an external DAC and applied to C4 through a filter consisting of R9 and C8. The filter removes noise from the external input, while slowing the transitions somewhat. In normal operation, transistor Q3 is turned on by writing a logic 1 to U3-12, shorting C4 to ground. Voltage variations at P1-10 will then not create an undesired current at the electrometer input.

8. Bead power supply

The bead power supply has four sections: a regulated bias voltage source, a linear current regulator, a DAC to set the current, and a switching pre-regulator for the current regulator. R26, R27, and AR4 (pins 8-10) provide a stable, low impedance source of -4V to bias the bead. C25 keeps switching supply noise out of AR4, and R28 prevents C25 from destabilizing AR4.

DAC U6, together with AR4, generates a voltage which varies between 0 and -10V with 12-bit resolution. C29 eliminates DAC output noise due to digital sources. The Thevenin equivalent of the DAC output (through R21 and R15), combined with the -10V reference (through R16), is a generator which varies between -4V and -10V, with a source resistance of 6K. This equivalent generator drives the inverting input of AR3 and resistor R14. Ignoring R28 for the moment, the other end of R14 is held at -4V, irrespective of the bead current. AR3 will adjust its output, which controls the bead current through Q4, to bring its noninverting input to the same voltage as the inverting input. The result is that R17 must have the same voltage drop across it as does R14. As the DAC setting is varied from 0 to 4095, this voltage drop goes from 0 to 572mV, and the current through R17 varies from 0 to 3.8A. Since the bead current switching supply

is floating, all of the current through R17 also flows through the bead (connected across J2-2&3), and the DAC controls the bead current. C19 suppresses digital noise.

To keep the power dissipation in Q4 low, a switching pre-regulator holds the voltage across Q4 at 390mV. U7 is operated in the flyback mode, alternately connecting T1-4 to ground and then opening the connection. When T1-4 is grounded, CR3 is reverse-biased, and the current in the primary of T1 rises linearly. When the output switch in U7 opens, the voltages at T1-4 and T1-9 rise rapidly, turning on CR3, and transfering the energy stored in the primary into C22 and C23. CR4 and VR1 clamp the voltage spike across the primary, absorbing the energy stored in the leakage inductance of T1. C30 supplies the high current pulses required when U7 turns on.

The voltage across Q4 is amplified by AR4 (pins 12-14), which is configured as a differential amplifier by R22-R25. U7 adjusts its duty cycle to maintain 1.24V at its feedback pin (U7-2), which occurs when the voltage across Q4 is 390mV. C32 provides a high-frequency feedback path to preserve loop stability. When the bead is unplugged, the feedback loop is opened, and the regulator would continue to increase its output voltage indefinitely. This is prevented by CR5, which closes the loop and holds the output voltage steady when it rises to 1.9V. (Normal output voltages are always below ground, since the bead resistance is between 0.5 and 0.75Ω.) CR6 prevents U7 from being latched up by driving pin 2 negative during a transient or fault condition, and R31 limits the current from AR4 when either CR6 or CR5 is conducting. C33 and R32 provide loop frequency compensation, and CR7 allows the supply to be turned off by setting U3-5 low.

9. Log of revisions and file identification

Rev. 1 9/12/95

File: ENGRSERV:\3800ELEC\DOC\Tsdcd.doc

Author: D. DeFord

Revised by: D. DeFord